REMARKS

Claims 1-26 are pending.

35 U.S.C. § 102 Rejections

In the present Office Action, claims 1-23 stand rejected under 35 U.S.C. § 102 as being anticipated by the newly cited reference U.S. Patent No. 6,192,458 (hereinafter "Arimilli"). Applicant has reviewed the rejections and the newly cited art, and appreciates the examiner's careful consideration of the matter. However, after review, Applicant believes the claims recite features which are neither taught nor suggested. Accordingly, Applicant respectfully traverses the above rejections and requests reconsideration in view of the following discussion.

By way of preface, the claimed invention is generally directed to a method and mechanism for rapidly identifying particular needed sub-blocks of a transfer request. To that end, a transfer request corresponding to a given block is received, the transfer request comprising an address and a mask which indicates which of the sub-blocks are required as part of the request. For example, a selection of non-contiguous sub-blocks may be identified by the mask as needed for the transfer request. Consequently, the present claims recite that the transfer request includes not only an address, but also a "mask". Given the nature of the presently claimed invention, the mask is not simply an address. As recited in claim 1, the method includes:

> "receiving a transfer request which corresponds to a block of data . . . said transfer request comprising an address and a mask which indicates which of said sub-blocks are required as part of the request;
>
> generating a different address for each of said sub-blocks in response to receiving the transfer request"

As seen from the above, the claim recites (1) receiving the transfer request which includes an address and a mask, and (2) generating a different address for each of the

sub-blocks in response to receiving the transfer request. Generating the addresses for the sub-blocks is necessary for the presently claimed invention, because the transfer request includes a mask to identify which of the sub-blocks are needed.

In contrast to the above, Arimilli merely discloses a cache addressing scheme. The address disclosed by Arimilli includes a Tag portion, Index portion, and Byte portion. For example, Arimilli discloses:

> "FIG. 3 depicts a cache directory addressing scheme for a 32 bit data processing system using a two-way set associative cache upgradeable from 1 MB to 2 MB. The 1 MB cache directory addressing configuration employs a 64 byte cache line. A cache line is the block of memory which a coherency state describes, also referred to as a cache block. When addressing a 1 MB cache, bits 26-31 (6 bits) of the address specify an intra-cache line address, bits 13-25 (13 bits) of the address are utilized as an index to a set of two cache lines in the cache directory and the cache memory, and bits 0-12 (13 bits) of the address are utilized as the cache line address tag to identify a particular cache line within the set of two. The index field specifies a row or congruence class within the cache directory and memory containing a set of two cache lines, the address tag field identifies a member of the specified congruence class (i.e. a particular cache line within the set of two cache lines), and the intra-cache line address field allows a particular byte to be selected from the identified congruence class member (cache line).
>
> The 2 MB cache directory addressing configuration employs a 128 byte cache line with bits 25-31 (7 bits) of the address determining an intra-cache line address, bits 12-24 (13 bits) of the address being utilized as an index to the cache directory and the cache, and bits 0-11 (12 bits) of the address being utilized as the cache line address tag." (Arimilli, col. 1, lines 35-60). (emphasis added).

As can be seen from the above, Arimilli merely discloses using 6 bits to address one of 64 bytes, or 7 bits to address one of 128 bytes. Such a disclosure is not equivalent to the recited. Even were one to equate the intra-cache line address of Arimilli with the recited mask, which Applicant does not agree with, there is clearly no disclosure of "generating a different address for each of said sub-blocks in response to receiving the

transfer request." In the present Office Action, the bytes of Arimilli are equated with the recited sub-blocks. Accordingly, an equivalent disclosure in Arimilli may be generating a different address for each of the 64 (or 128) bytes in response to receiving the request. In other words, the generation of 64 different address in response to the request. Clearly, there is no such disclosure or suggestion.

The remaining features are similarly absent from the cited art. For example, as presently claimed, after generating different addresses for each of the sub-blocks, the required sub-blocks are detected and only those generated addresses which correspond to the required sub-blocks are utilized.

In view of the above discussion, it is believed apparent that the presently claimed invention and the cited disclosures are quite distinct. Accordingly, all of the independent claims (each of which includes the features discussed above) are patentably distinguished for at least these reasons.

Other non-disclosed features are included in the dependent claims as well. For example, claim 3 recites the mask includes a separate bit for each of the sub-blocks, and the value off a single bit indicates whether a corresponding sub-block is required. In contrast, Arimilli discloses either a 6 or 7 bit address to identify one of 64 or 128 bytes, respectively. Applicant submits these are quite distinct and are not equivalent.

Further, claim 5 recites concurrent generation of the sub-block addresses. As noted in the discussion above, Arimilli does not disclose the generation of different addresses as recited in claim 1. Claim 6 recites "selecting a first address". Applicant finds no such feature disclosed in the Arimilli. With respect to claim 7, Arimilli does not disclose "masking off said first bit". In contrast, Arimilli merely discloses a different address is used to address a different byte.

Applicant believes the application to be in condition for allowance. However, should the examiner believe issues remain which would prevent its allowance, the below

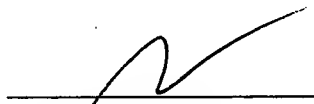
signed representative requests a telephone interview at (512) 853-8866 in advance of the deadline for replying to the present Office Action to facilitate a more speedy resolution.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-95300/RDR.

Respectfully submitted,



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